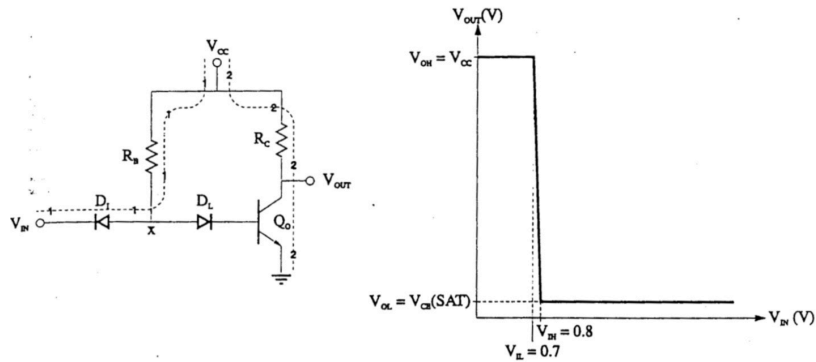


## Chapter 6 - Diode Transistor Logic - DTL

### Basic DTL Inverter.

\* This family of logic circuits was introduced to overcome the low fan-out of RTL for  $V_{out} = V_{OH}$



Output high voltage  $\equiv V_{OH}$

\* For  $V_{in}$  low  $D_I$  is forward biased

$$V_x = V_{in} + V_{D,I(ON)} < V_{D,L(ON)} + V_{BE,0(FA)}$$

This not large enough to turn on  $D_L$  &  $Q_0$  therefore  $Q_0$  is cutoff and  $I_{RC} = I_C = 0$

$$V_{out} = V_{CC} - I_{RC} R_c = V_{CC} = V_{OH}$$

Input low Voltage  $\equiv V_{IL}$

\* Increasing  $V_{in}$  to the point where  $Q_0$  just turns on is advised when

$$V_{in} = V_{BE(FA)} = V_{IL}$$

Output low voltage  $\equiv V_{OL}$

\* Increasing  $V_{in}$  (and therefore  $V_x$ ) further eventually drives  $Q_0$  into saturation giving

$$V_{out} = V_{CE(sat)} = V_{OL}$$

Input High Voltage  $\equiv V_{IH}$

Transistor  $Q_0$  enters saturation at

$$V_{in} = V_{BE,0(sat)} + V_{D,L(ON)} - V_{D,I(ON)} = V_{BE(sat)} = V_{IH}$$

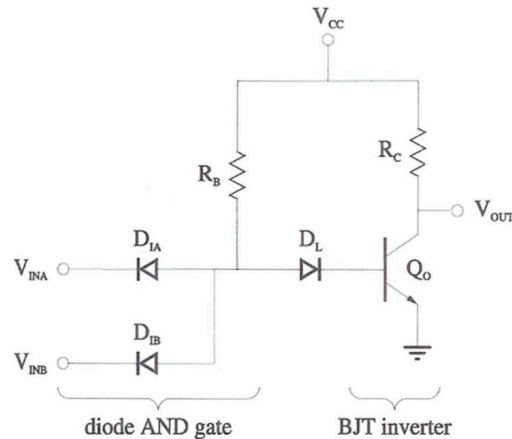
\* Resistor  $R_B$  must be chosen small enough such that  $Q_0$  is in saturation when

$$V_x = V_{BE(sat)} + V_{D(on)}$$

\* Since  $V_{IL}$  &  $V_{IH}$  differ only by  $V_{BE(sat)} - V_{BE(FA)}$  the transition width between output high & low logic states is quite abrupt

### Basic DTL NAND Gate

\* Addition of another input diode resembles a diode AND gate connected to a BJT inverter.



### Modified DTL

#### Additional Level-Shifting.

\* An additional level shifting diode  $D_2$  has been added in series with  $D_1$  to shift the logic level transition by  $V_{D(on)}$  on the VTC input voltage axis. This improves the low noise margin  $NM_L$  while still exhibiting an acceptable high noise margin  $NM_H$ .

\* The additional level-shifting diode also avoids the problem of  $Q_0$  turning on before  $V_{in}$  reaches 0.7V.

\* The addition of  $D_2$  increases  $V_{IL}$  &  $V_{IH}$  by  $V_{D(on)} = 0.7V$

### Discharge Path

\*  $R_D$  &  $-V_{EE}$  at the base of  $Q_0$  provide a path for discharge of the stored base charge of  $Q_0$  when switched from saturation to cutoff.

\* The need for an additional source voltage can be avoided by simply taking  $-V_{EE}$  to be ground and using a smaller valued resistance for  $R_D$ .

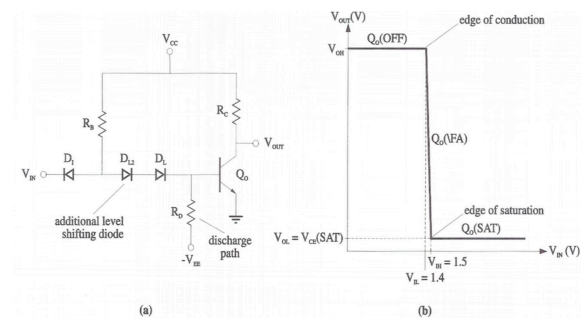


FIGURE 6.3 Modified DTL: (a) Circuit with additional level-shifting diode and discharge path, (b) Voltage transfer characteristic

## Transistor Modified DTL

\*The fan-out of DTL circuits can be further improved by replacing the level-shifting diode  $D_L$  with a BJT  $Q_L$  & splitting  $R_B$  into two resistors  $\rho R_B$  &  $(1-\rho)R_B$ , whose sum is  $R_B$

\*This circuit improves fan-out by  $Q_L$  providing more base-driving current to  $Q_O$  allowing  $Q_O$  to sink more current from an output load.

\*If  $\rho = 1$  the  $J_{BC}$  of  $Q_L$  is shorted causing  $Q_L$  to act as a diode.

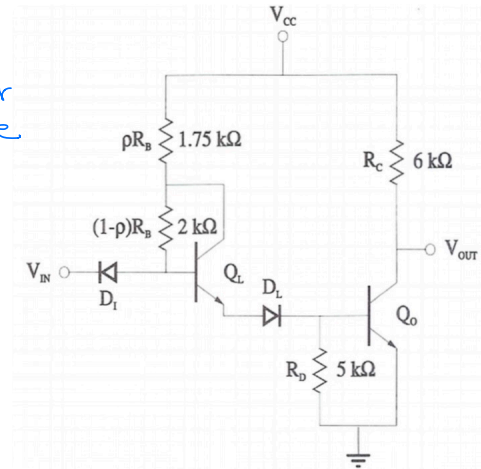


FIGURE 6.4 Transistor Modified DTL (930 Series)

TABLE 6.1 Purpose of DTL Elements

| Element       | Purpose  |
|---------------|--|
| $D_I$         | Input diode, limits $I_{IL}$ , and provides ANDing   |
| $\rho R_B$    | Limits $I_{IL}$  |
| $(1-\rho)R_B$ | Self biases $Q_L$  |
| $Q_L$         | Base-emitter level-shifting for shift of transition width and provides base driving current to $Q_O$ |
| $D_L$         | Level-shifting diode for shift of transition width   |
| $R_D$         | Provides discharge path for saturation stored charge removal from base of $Q_O$                      |
| $Q_O$         | Output inverting BJT and output low driver for current sinking pull-down                             |
| $R_C$         | Passive current sourcing pull-up   |

TABLE 6.2 State of Diodes and BJTs for Output High and Low Levels

| Element | $V_{OH}$ | $V_{OL}$       |
|---------|----------|----------------|
| $D_I$   | On       | Cutoff         |
| $Q_L$   | Cutoff   | Forward active |
| $D_L$   | Cutoff   | On             |
| $Q_O$   | Cutoff   | Saturated      |

### Example 6.1 VTC of Transistor Modified DTL

Determine the VTC of the transistor modified DTL inverter in Figure 6.4. Use  $V_D(\text{ON}) = 0.7 \text{ V}$  for the diodes and  $V_{BE}(\text{FA}) = 0.7 \text{ V}$ ,  $V_{BE}(\text{SAT}) = 0.8 \text{ V}$ , and  $V_{CE}(\text{SAT}) = 0.2 \text{ V}$  for the BJTs.

$$V_{OH} = V_{CC} = 5 \text{ V}$$

$$V_{OL} = V_{CE,0}(\text{sat}) = 0.2 \text{ V}$$

$Q_O$  turns on at

$$V_{IL} = V_{BE,0}(\text{FA}) + V_{D,L}(\text{ON}) + V_{BE,L}(\text{FA}) - V_{D,I}(\text{ON})$$

$$= 2V_{BE}(\text{FA}) = 2(0.7) = 1.4 \text{ V}$$

and saturates at  $V_{IH} = V_{BE,0}(\text{sat}) + V_{D,L}(\text{ON}) + V_{BE,L}(\text{FA}) - V_{D,I}(\text{ON})$

$$V_{IH} = V_{BE}(\text{sat}) + V_{BE}(\text{FA}) = 0.8 + 0.7 = 1.5 \text{ V}$$

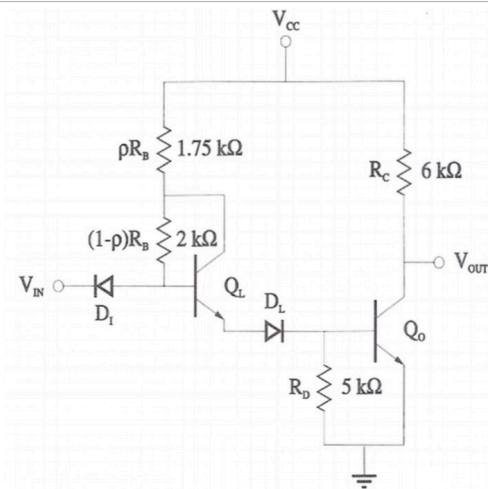


FIGURE 6.4 Transistor Modified DTL (930 Series)

\*Note that  $Q_L$  can never saturate because the voltage polarity for the resistor  $(1-\rho)R_B$  maintains a negative  $V_{BC,L}$  for  $Q_L$ .

### DTL NAND Gate

\*For any input low

$$V_x = V_{in}(\text{low}) + V_{D_L}(\text{on})$$

$$< V_{BE,L}(\text{FA}) + V_{D_L}(\text{on}) + V_{BE,O}(\text{FA})$$

$\therefore Q_O$  is cutoff

$$V_{out} = V_{OH} = V_{cc}$$

\*for all inputs high

$V_x$  is high allowing  $Q_O$  to saturate (provided that  $\rho R_B$  is chosen properly.)

$$V_{out} = V_{CEO}(\text{sat}) = V_{OL}$$

therefore:

The DTL logic family provides the logical NAND operation

### DTL Fan-out

\*when  $V_{out} = V_{OH}$  for the driving gate reverse biases the input diodes of all load gates such gates sink very little current & hence do not impose a fan-out restriction.

\*The maximum fan-out is obtained by determining how much output current  $I_{OL}$  the driving gate can sink from multiple identical output gates

$$N I_{IL} = I_{OL}$$

$$N = \frac{I_{OL}}{I_{IL}}$$

\*To determine  $N$  we use the following figure, which shows one of the load gate explicitly with  $V_{out} = V_{in} = V_{OL}$

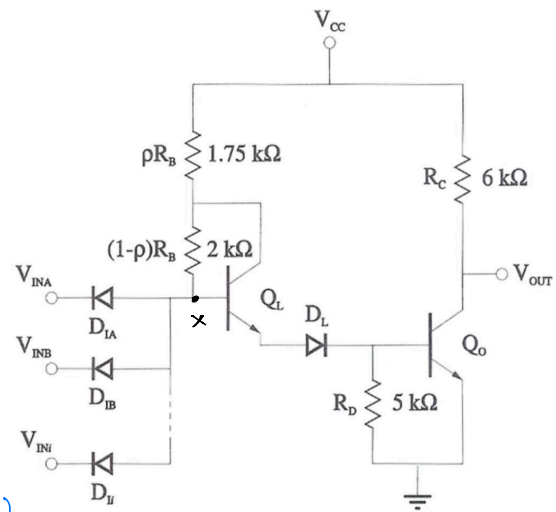
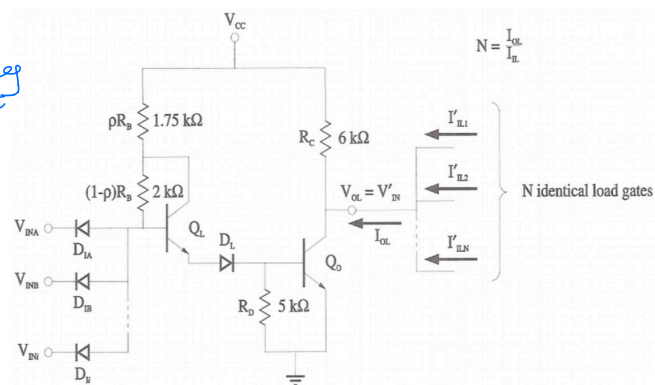


FIGURE 6.5 930 Series DTL NAND Gate





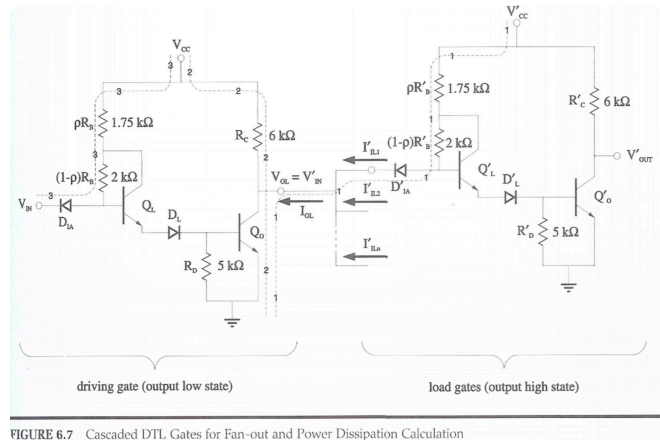


FIGURE 6.7 Cascaded DTL Gates for Fan-out and Power Dissipation Calculation

Input low current  $\equiv I_{IL}$

$$I'_{PRB} = I_{IL} = \frac{V_{CC} - V_{D_i(ON)} - V_{CE,o(sat)}}{pR'_B + (1-p)R'_B}$$

$$= \frac{V_{CC} - V_D(ON) - V_{CE}(sat)}{R_B} = I_{RB}$$

Output low current  $\equiv I_{OL}$

$$I_{OL} = I_{C,o(sat)} - I_{RC}$$

$$I_{RC} = \frac{V_{CC} - V_{CE,o(sat)}}{R_C}$$

$$I_{C,o(sat)} = \sigma_{OL} \beta_f I_{B,o(sat)}$$

\* For maximum fan-out we consider operation at the edge of saturation where  $\sigma = 1$

$$I_{C,o(sat)} = I_{C,o(EOS)} = \beta_f I_{B,o(EOS)}$$

$$I_{B,o} = I_{E,L} - I_{RD}$$

$$I_{RD} = \frac{V_{BE,o(sat)}}{R_D}$$

\* The emitter current of  $Q_L$  is found by analyzing the portion of the driver gate including  $V_{CC}$ ,  $pR_B$ ,  $(1-p)R_B$ ,  $Q_L$ ,  $D_L$ , &  $Q_o$  as shown in figure to the right

\* Considering  $Q_L$  &  $(1-p)R_B$  as a super-node the current through  $pR_B$  is equal to the emitter current of  $Q_L$ .

$$I_{E,L} = \frac{V_{CC} - V_{BE,L(FA)} - V_{D,L(ON)} - V_{BE,o(sat)}}{pR_B}$$

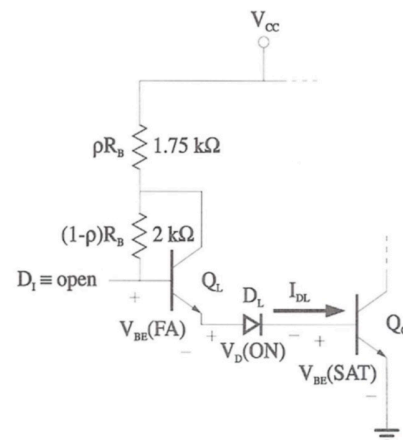


FIGURE 6.8 Portion of DTL Driving Gate for Fan-out Analysis and Power Dissipation Analysis

### Example 6.2 DTL Fan-Out

Calculate the fan-out for the DTL inverter of Figure 6.7 considering the circuit in Figure 6.7 and the sub-circuit in Figure 6.8. Let  $\beta_F = 49$ ,  $V_{BE}(FA) = 0.7$  V,  $V_{BE}(SAT) = 0.8$  V, and  $V_{CE}(SAT) = 0.2$  V for the BJTs and  $V_D(ON) = 0.7$  V for the diodes. Also, use  $\sigma_{OL} = 0.85$  for the output low state.

$$N = \frac{I_{OL}}{I_{IL}}$$

$$I_{IL} = \frac{V_{CC} - V_D(ON) - V_{CE}(SAT)}{R_B}$$

$$= \frac{5 - 0.7 - 0.2}{3.75k} = 1.09 \text{ mA}$$

$$I_{OL} = I_{CQ}(SAT) - I_{PC}$$

$$I_{PC} = \frac{V_{CC} - V_{CEQ}(SAT)}{R_C}$$

$$= \frac{5 - 0.2}{6k\Omega} = 800 \mu A$$

$$I_{CQ}(SAT) = \sigma_{OL} \beta_F I_{BQ}(SAT)$$

$$I_{BQ}(SAT) = I_{E1} - I_{RD}$$

$$I_{RD} = \frac{V_{BEQ}(SAT)}{R_D} = \frac{0.8}{5k} = 160 \mu A$$

$$I_{E1} = \frac{V_{CC} - V_{BE1}(FA) - V_{D1}(ON) - V_{BEQ}(SAT)}{R_B} = \frac{5 - 0.7 - 0.7 - 0.8}{1.75k} = 1.60 \text{ mA}$$

$$I_{BQ}(SAT) = 1.60 \text{ mA} - 160 \mu A = 1.44 \text{ mA}$$

$$I_{CQ}(SAT) = 0.85 \times 49 \times 1.44 \text{ mA} = 60 \text{ mA}$$

$$I_{OL} = 60 \text{ mA} - 800 \mu A = 59.2 \text{ mA}$$

$$N = \frac{59.2 \text{ mA}}{1.09 \text{ mA}} = 54.3$$

\* The fan-out of this DTL gate is 54

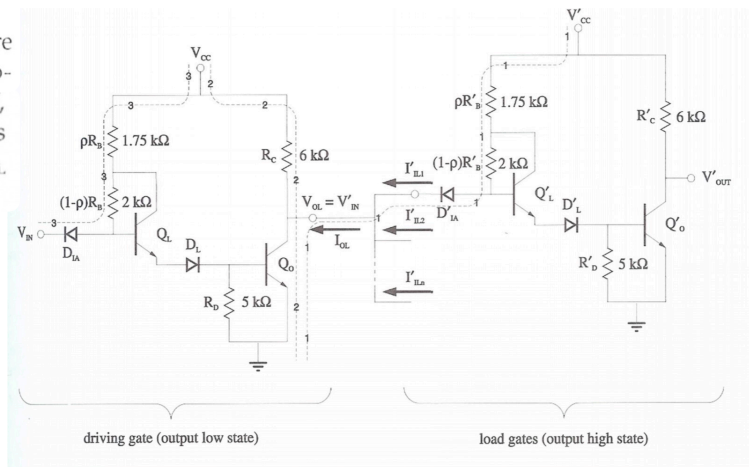


FIGURE 6.7 Cascaded DTL Gates for Fan-out and Power Dissipation Calculation

For finding  $p$

$$\frac{pR_B}{(1-p)R_B} = \frac{1.75k}{2k}$$

$$2p = 1.75 - 1.75p$$

$$3.75p = 1.75$$

$$p = \frac{1.75}{3.75} = 0.467$$

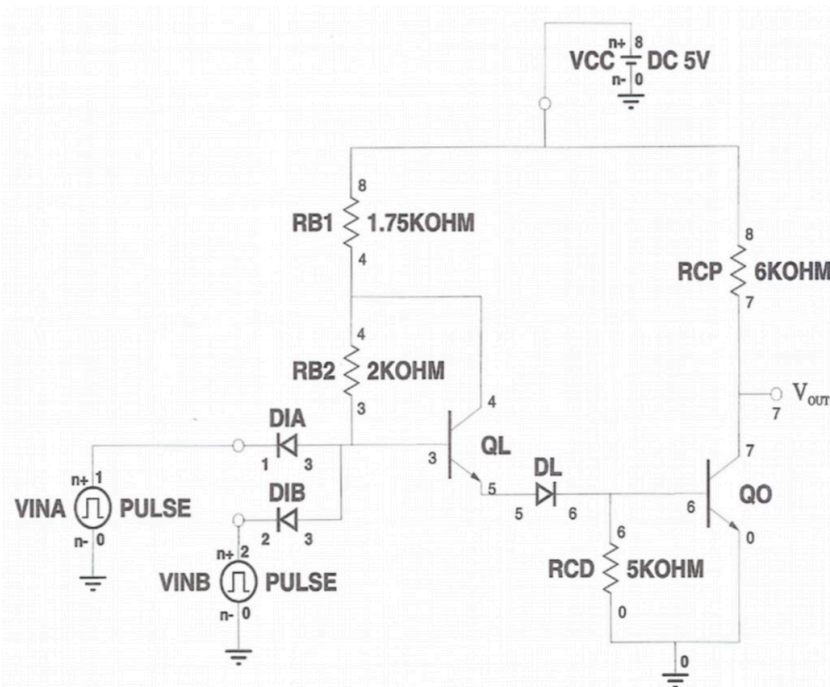


### Example 6.3 DTL Power Dissipation

Calculate the average power dissipation for the DTL gate in Example 6.2.

$$\begin{aligned} P_D(\text{avg}) &= \frac{I_{cc}(\text{OH}) + I_{cc}(\text{OL})}{2} V_{cc} \\ &= \frac{I_{PRB}(\text{OH}) + I_{PRB}(\text{OL}) + I_{cc}(\text{OL})}{2} \cdot V_{cc} \\ &= \frac{1.09\text{mA} + 1.60\text{mA} + 800\mu\text{A}}{2} (5) \\ &= 8.73\text{mW} \end{aligned}$$

### DTL SPICE Simulation



DTL Gate with SPICE Labelings

